Design Space Exploration in High-Level Synthesis

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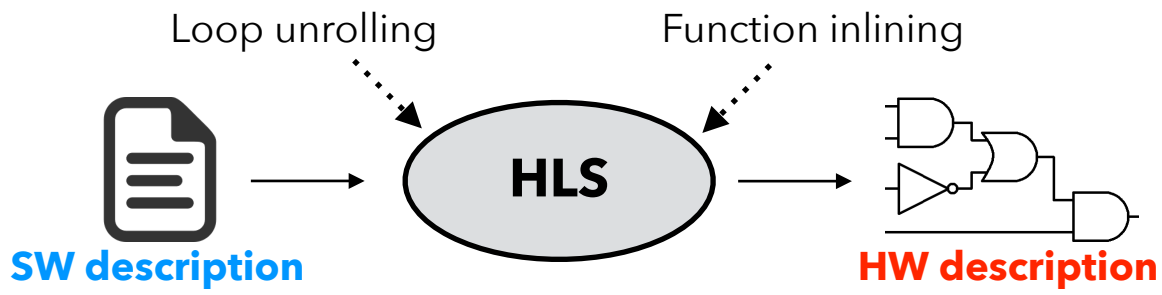
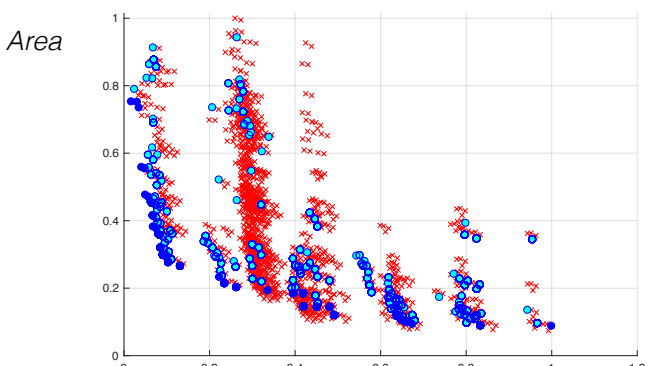
The Design Space Exploration Problem:

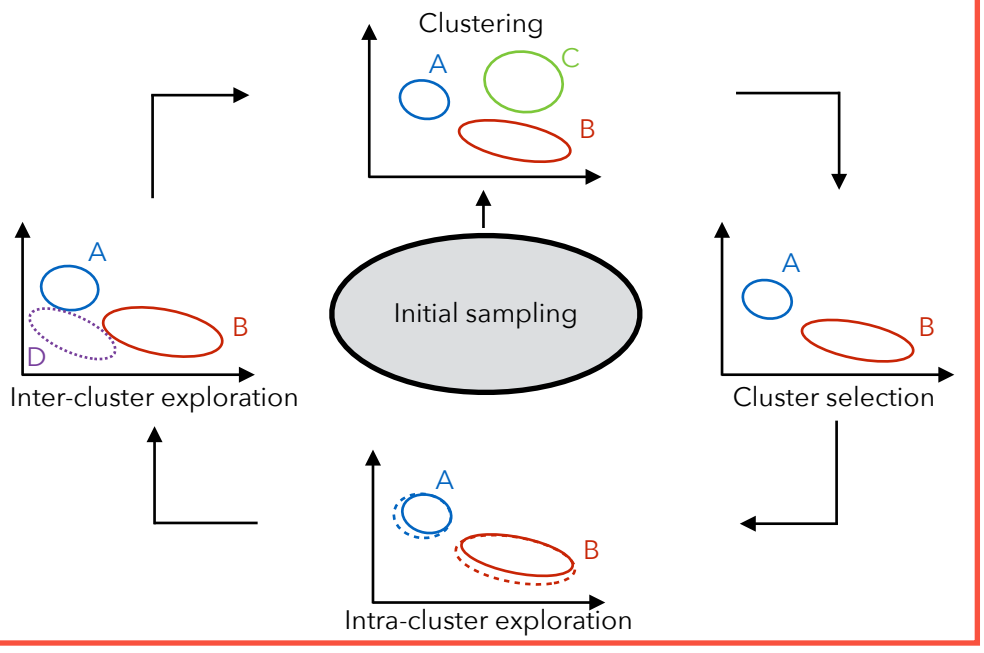




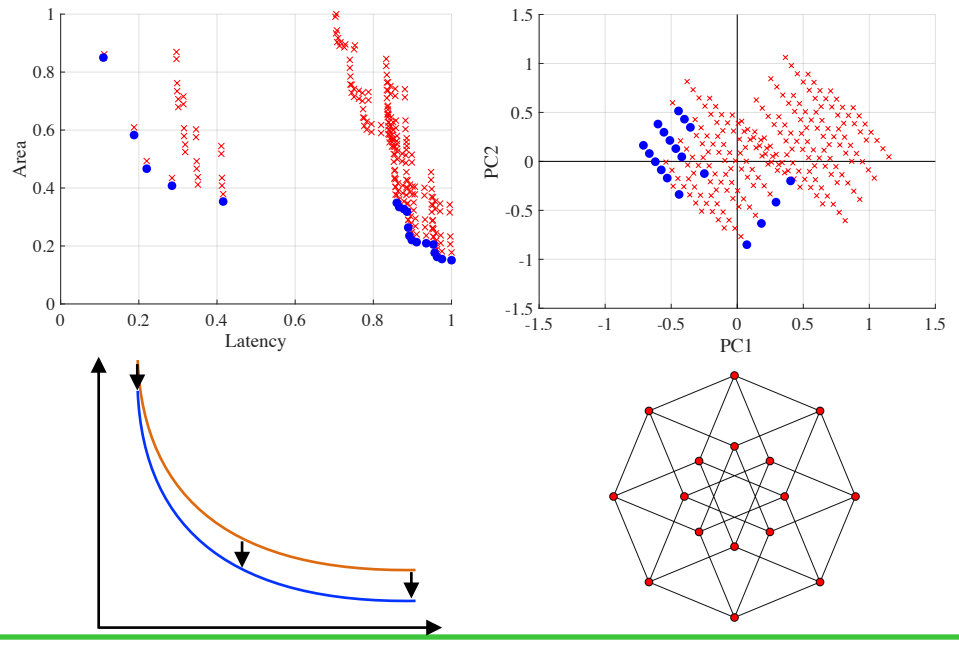
Different approaches:

- Model-based, designers knowledge is used to imitate the HLS process.
- Black-box-based, learning and refinement based strategies are used to guide the DSEs.

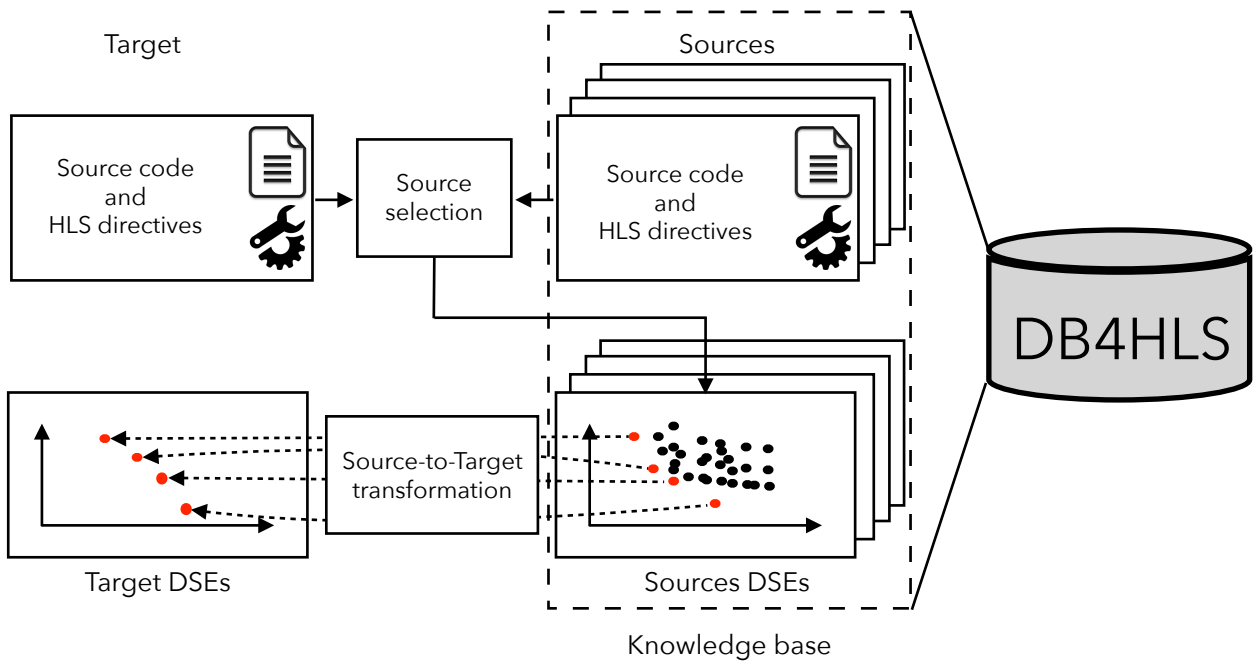
Cluster-based heuristics to navigate the design space [1].



Reshaping the design space to identify Pareto-solution properties [2].



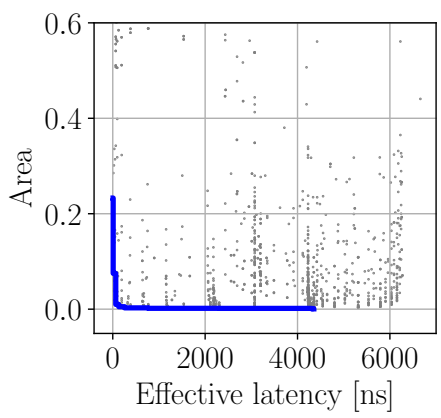
Leveraging prior knowledge [3] & a DB of DSEs [4].



Results

	Prior knowl. [3]	Lattice [2]	Cluster [1]	RF-TED [5]	Zhong [6]
< 200	7	36	37	155	NA
< 700	10	64	64	391	19
< 1800	22	230	290	1588	31
< 6000	19	460	460	1903	32
< 16000	NA	NA	NA	NA	35
< 32000	38	NA	NA	NA	NA

ADSR = 0.04



References:
[1] Ferretti, L., et al., 2018. Cluster-based heuristic for high level synthesis design space exploration. *IEEE Transactions on Emerging Topics in Computing (TETC).*
[2] Ferretti, L., 2018. Lattice-traversing design space exploration for high level synthesis. *IEEE 36th International Conference on Computer Design (ICCD) .*
[3] Ferretti, L., et al,. 2020. Leveraging Prior Knowledge for Effective Design-Space Exploration in High-Level Synthesis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).*
[4] Ferretti, L., et al., 2021. DB4HLS: A Database of High-Level Synthesis Design Space Explorations. *arXiv preprint arXiv:2101.00587.*
[5] Liu, H.Y. and Carloni, L.P., 2013. On learning-based methods for design-space exploration with high-level synthesis. Design Automation Conference (DAC).
[6] Zhong, G., et al., 2014. Design space exploration of multiple loops on FPGAs using high level synthesis. *IEEE International conference on computer design (ICCD).*